EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 01245350
PUBLICATION DATE : 29-09-89

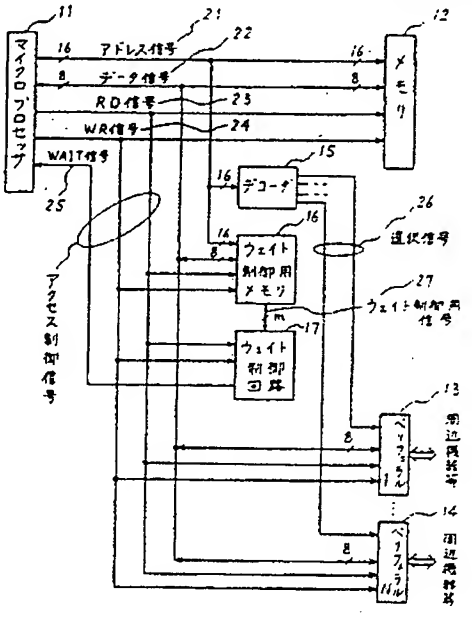
APPLICATION DATE : 28-03-88
APPLICATION NUMBER : 63075005

APPLICANT : NEC CORP;

INVENTOR : MUROI KIYOSHI;

INT.CL. : G06F 13/42

TITLE : WAIT CONTROL SYSTEM



ABSTRACT : PURPOSE: To directly apply the same circuit to various microcomputer apparatuses by providing the title system with a wait controlling memory for outputting a wait controlling signal and a wait control circuit for outputting a WAIT signal.

CONSTITUTION: The wait controlling memory 16 inputs an address signal and outputs '1' e.g. as a wait controlling signal 27 when one-time slot width is required for the wait cycle of addresses allocated to peripherals 13, 14, or '2' when two-time slot width is required. The data can be read/written from/in a microprocessor 11. A wait controlling circuit 17 generates a WAIT signal 25 corresponding to a necessary wait cycle in accordance with an access control signal. In said constitution, the memory 16 and the circuit 17 can be independent of the constitution of the peripherals. Thereby, the same circuit can be directly applied to various microcomputer application apparatuses. In addition, the number of wait operations to be inserted into the peripherals 13, 14 can be optionally set up and changed.

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